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EXAMINER	
JACOBSON, TONY M	
ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 09/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,763	LI ET AL.	
	Examiner	Art Unit	
	Tony M. Jacobson	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 and 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al. (US 5,442,709) in view of Patel et al. (US 5,479,449) and Whikehart et al. (US 5,936,438).

3. Regarding claim 1, Vogt et al. disclose in Fig. 1, a decoder having an input signal (1) and a first output signal (13), comprising a multiplier (15 or 15a) for multiplying a predetermined value (16) by the input signal to generate an intermediate signal, wherein the input signal has a pilot signal component and wherein the pilot signal component in the intermediate signal is a predetermined lower frequency than the pilot signal component in the input signal (see column 4, lines 21-36); a filter (18 or 17) for receiving the intermediate signal and for providing the pilot signal as an output; a circuit (21, see Fig. 2) coupled to the filter for receiving the pilot signal component (SPC1 and SPC2) from the outputs of said filters, the predetermined lower frequency of the pilot signal being sufficiently low to permit said circuit to determine an approximate phase of the pilot signal component of the intermediate signal and generate at least one trigonometric function (G38c and G38s) using the approximate phase of the pilot signal

component of the intermediate signal (see column 4, line 18 -column 5, line 18); means (4 and 5 of Fig. 1) for using the at least one trigonometric function to phase align a first data component (L-R) of the input signal with a second data component (L+R) of the input signal and provide a phase aligned first data component; and means (7, 9, and 11) for using the phase-aligned first data component to generate the first output signal (R at element 13 of Fig. 1).

4. Vogt et al. do not disclose that the circuit coupled to the filter(s) for receiving the pilot signal component from the output(s) of the filter(s) and generating at least one trigonometric function using the determined approximate phase of the pilot signal component is a phase lock loop; instead the circuit of Fig. 2 performs that function in a more direct manner by forming the product of and the difference of the squares of the two quadrature-phase pilot error signals SPC1 and SPC2 (corresponding to the cosine and sine of the phase error between the received pilot signal and the reference pilot signal applied to multiplier 15) as described at column 4, lines 39-64. Circuit 21 of Fig. 2 functions to receive a quadrature-phased pair of signals SPC1 and SPC2, representing the cosine and sine, respectively, of the phase error between the received pilot signal and a reference signal, and produce signals G38c and G38s which are proportional to the cosine and sine, respectively, of twice the phase error between the received pilot signal and the reference pilot signal applied to multiplier 15. In other words, circuit 21 doubles the phase (and thus frequency) of the sinusoidal error signals SPC1 and SPC2.

5. Patel et al. disclose in Fig. 5, a digitally-controlled oscillator (270) which in combination with quadrature synchronous detector 250 forms a phase-locked loop using sine and cosine lookup tables (271 and 272) to generate sine and cosine function outputs at the same frequency as, and phase aligned with a quadrature-phased pair of input signals. In the embodiment of Fig. 5, Patel et al. include a second pair of sine and cosine lookup tables (2701 and 2702) for providing phase-adjusted sine and cosine signals to in-phase synchronous detector 230 to compensate for the delay introduced into the carrier signals by bandpass filters 52 and 53. It was well known in the digital signal processing art at the time the present invention was made to obtain synchronized harmonically-related signals from lookup tables by either multiplying the lookup address/index into one table by a constant (modulo the number of samples per period) to form a second index into the same or an identical table for generating a higher frequency waveform, or by providing a second lookup table having multiple periods of the desired waveform stored in the same number of samples as a single period of a lower-frequency waveform stored in a first table. Whikehart et al. describe at column 2, line 63 –column 3, line 55, both of these methods for obtaining different harmonically-related sinusoidal signals. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to substitute the phase-locked loop of Patel et al. for circuit 21 of Figs. 1 and 2 of Vogt et al., with look-up tables 2701 and 2702 modified to store two cycles of the sine and cosine waveforms in the same number of samples as single cycles are stored in look-up tables 271 and 272, or alternatively, to multiply the indices into look-up tables 2701 and 2702 by two, to produce a pair of

phase-adjusted output signals synchronized at twice the frequency of the input quadrature-phased signals, producing sine(2*θ + α) and cosine(2*θ+ α) lookup table outputs as an alternative to the circuit (21) disclosed by Vogt et al. in order to avoid the prior art.

6. Regarding claim 2, in the decoder of Vogt et al., unmodified or modified according to the teachings of Patel et al. and Whikehart et al. as described above, the at least one trigonometric function includes a sine function and a cosine function.

7. Regarding claims 3 and 4, Vogt et al. disclose in Fig. 1 and at column 4, lines 18-26 that the predetermined value is a cosine value retrieved from a table (16).

8. Regarding claims 5 and 6, the decoder of Vogt et al. has a second output (12), the first output signal (13) is a right stereo channel and the second output signal is a left stereo channel, the first data component is a difference between a left channel and a right channel, and the second data component is a summation of the left channel and the right channel.

9. Regarding claim 7, the means for using the phase aligned first data component to generate the first output signal in the decoder of Vogt et al. comprises a stereo blender (elements 7, 8, 9, 10, 11, and 22; see column 4, lines 7-10).

10. Regarding claim 11, Vogt et al. disclose that the system is used for decoding a multiplex signal in a stereo receiver of VHF/FM stereo broadcasting (column 1, lines 18-23 and column 3, lines 3-6).

11. Regarding claims 12 and 13, the predetermined value of Vogt et al. is nominally 19-kHz, the same as the nominal frequency of the pilot signal component in

the input signal; however since it is independently generated in a free-running oscillator, it is approximate to, but not equal to, a frequency of the pilot signal component in the input signal and within 3-kHz (probably within a few Hz) of the frequency of the pilot .

12. Regarding claims 14 and 15, in the decoder of Vogt et al., modified according to the teachings of Patel et al., the system comprises a decimator (19 or 20) coupled between said filter(s) and said phase-locked loop, and said decimator reduces a frequency (the sampling frequency) of the intermediate signal.

13. Regarding claim 16, Vogt et al. disclose at column 4, lines 33-36 that because the frequency of the signals output by low-pass filters 17 and 18 is much lower in comparison to the pilot signal, the sampling rate is reduced at 19 and 20 in order to "save significant expense in the network 21". Although Fig. 1 implies that the signals are decimated by factors of 23 and 24, respectively, one of ordinary skill in the art would reasonably conclude that this was not the intended meaning. Inspection of Fig. 1 in an equivalent disclosure of US patent 5,696,830 by Chahabadi et al. (including Vogt) verifies that this is indeed the case, and the symbols "23" and "24" were intended as reference characters identifying the output signals "SPC1" and "SPC2" of decimators 19 and 20, respectively. Although Vogt et al. do not explicitly disclose the factor by which the sampling rate is reduced by decimators 19 and 20, since it is disclosed at column 4, lines 26-28 that low-pass filters 17 and 18 limit their output frequencies to about 70 17-Hz, whereas in the present invention, the signal output by low-pass filter 372 has a nominal frequency of 1-kHz, an even greater sampling-rate reduction could be utilized in the system of Vogt et al., modified according to the teachings of Patel et al. It would have

been obvious to one of ordinary skill in the art would at the time the present invention was made to use the maximum possible reduction factor, commensurate with the sample rate requirements of the phase-locked loop, in order to reduce the computational load or expense in the phase-locked loop.

14. Regarding claim 17, in the system of Vogt et al., modified according to the teachings of Patel et al. and Whikehart et al. as described above, the phase-locked loop operates at a frequency less than one tenth a frequency of the input frequency (nominally 0-Hz, probably a few Hz at maximum).

15. Regarding claim 18, the system of Vogt et al., modified according to the teachings of Patel et al. and Whikehart et al. as described above in regard to claims 1-6, performs the method claimed, further generating an L+R signal from the input signal where L is a left channel and R is a right channel; generating an L-R signal from the input signal and using the first and second trigonometric functions; and using the L+R signal and the L-R signal to produce a left channel output signal and a right channel output signal.

16. Regarding claim 19, as described above regarding claim 1, Patel et al. disclose in Fig. 5 and at column 12, line 48 –column 13, line 19 that a predetermined phase correction constant (α) is added to the phase information of the input signal to produce a resultant phase value, wherein the predetermined phase correction is a function of a delay of a portion of the digital circuitry. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to apply this teaching to the

system of Vogt et al. in order to offset the differential delay between the paths of the pilot signal and the L-R signal.

17. Regarding claim 20, as described above regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to multiply the index into tables 2701 and 2702 of Fig. 5 of Patel et al. by two according to the teachings of Whikehart et al. to provide sine and cosine outputs from tables 2701 and 2702 having twice the phase and frequency of the outputs of tables 271 and 272 for application to multipliers 4 and 5 of Vogt et al.

18. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al. (US 5,442,709) in view of Patel et al. (US 5,479,449) and Whikehart et al. (US 5,936,438) as applied to claims 1-7 above, and further in view of Collier et al. (US 5,404,405).

19. Regarding claim 8, Vogt et al. disclose in Fig. 1 a first and a second filter (10 and 11) for providing first and second outputs, respectively; and combining circuitry (8 and 9) coupled to the first and second filters. The combining circuitry of Vogt et al. does not combine the first filter output and the second filter output to produce the first and second output signals; rather the Vogt et al. filter the outputs of the combining circuitry to produce the first and second output signals. Collier et al. disclose in Fig. 1, a similar decoder in which a first and second filter (40 and 42) provide outputs to combining circuitry (44 and 46) which combines the first filter output and the second filter output to produce the first and second output signals. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to place the

filters of Vogt et al. prior to the combining circuitry instead of following it, as taught by Collier et al. in order to reduce distortion in the combining circuitry by eliminating the non-baseband components from the signals prior to their application to the combining circuitry.

20. Regarding claim 9, as broadly as claimed, the filter coefficients of the first and second filters in the decoder of Vogt et al., modified according to the teachings of Patel et al., Whikehart et al., and Collier et al. as described above, are inherently selectable (by the system designer).

21. Regarding claim 10, Vogt et al. do not disclose the specific type of filters implemented in the system, other than stating that the system operates on digital signals by means of digital signal technology, as indicated at column 1, lines 40-61. Collier et al. disclose with regard to filters 8a, 8b, 8c, etc., composing filter 8, at column 2, lines 66-68 that these filters are implemented as FIR filters to assist in maintenance of phase coherence in the decoding process. Collier et al. further mention throughout the disclosure that filters 10, 16, 18, and 20 are FIR filters. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to use FIR filters prior to the combining circuitry of the system of Vogt et al., according to the teachings of Collier et al. in order to maintain phase coherence in the decoding process.

22. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al (US 5,442,709) in view of Collier et al. (US 5,404,405).

23. Regarding claim 21, Vogt et al. disclose in Fig. 1, a digital processing system performing a method of decoding an input signal containing information on a left channel L and a right channel R, comprising sampling (inherently) the input signal which has a pilot signal component; mixing the input signal with a predetermined value to provide an intermediate signal having the pilot signal component wherein a frequency of the pilot signal component of the intermediate signal is significantly lower than the pilot signal component of the input signal; filtering the intermediate signal to provide the pilot signal component of the intermediate signal as a filter output; determining an approximate phase of the pilot signal component of the intermediate signal and generating first and second trigonometric functions using the approximate phase of the pilot signal component of the intermediate signal; generating an L+R signal from the input signal; generating an L-R signal from the input signal and using the first and second trigonometric functions; combining the L+R and L-R signals to produce left and right unfiltered signals, and filtering the unfiltered left and right signals to produce filtered left and right output signals. The combining circuitry of Vogt et al. does not combine the first filter output and the second filter output to produce the first and second output signals; rather the filters of Vogt et al. filter the outputs of the combining circuitry to produce the first and second output signals. Collier et al. disclose in Fig. 1, a similar decoder in which a first and second filter (40 and 42) provide outputs to combining circuitry (44 and 46) which combines the first filter output and the second filter output to produce the first and second output signals. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to place the filters of

Vogt et al. prior to the combining circuitry instead of following it, as taught by Collier et al. in order to reduce distortion in the combining circuitry by eliminating the non-baseband components from the signals prior to their application to the combining circuitry.

24. Regarding claim 22, Vogt et al. do not disclose the specific type of filters implemented in the system, other than stating that the system operates on digital signals by means of digital signal technology, as indicated at column 1, lines 40-61. Collier et al. disclose with regard to filters 8a, 8b, 8c, etc., composing filter 8, at column 2, lines 66-68 that these filters are implemented as FIR filters to assist in maintenance of phase coherence in the decoding process. Collier et al. further mention throughout the disclosure that filters 10, 16, 18, and 20 are FIR filters. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to use FIR filters prior to the combining circuitry of the system of Vogt et al., according to the teachings of Collier et al. in order to maintain phase coherence in the decoding process.

25. Regarding claim 23, Vogt et al. disclose that the functional stages of the invention could be implemented by suitable programming of a digital signal processor (column 5, lines 32-38). It was well known in the art of digital signal processing at the time the present invention was made that digital signal processing could be implemented in hardware or software. Collier et al. disclose at column 5, lines 5-10 that the DSP functions, including FIR filters could be implemented in hardware or software. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to employ either hardware or software to implement the system of Vogt et al., modified according to the teaching s of Collier et al.

26. Regarding claim 24, in a software-implemented system as described above regarding claim 23, the filter coefficients are inherently software-modifiable.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

28. Chahabadi et al. (US 5,696,830) presents essentially the same disclosure as Vogt et al (US 5,442,709), but serves to clarify the labeling of decimators 19 and 20 of Fig. 1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tony M. Jacobson whose telephone number is (703) 305-5532. The examiner can normally be reached on Mon. -Fri. 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on (703) 305-4386. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

tmj

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PRIMARY EXAMINER